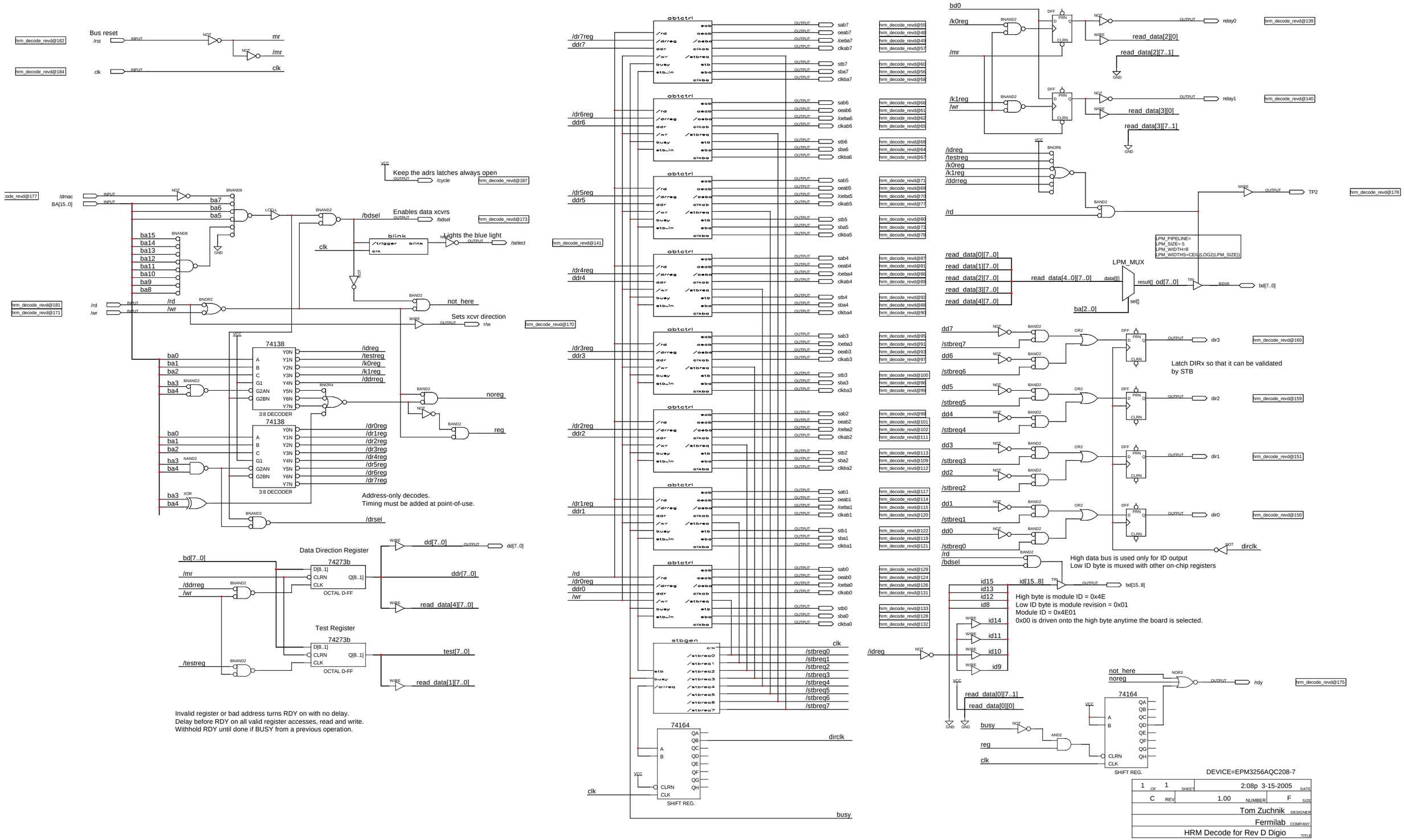
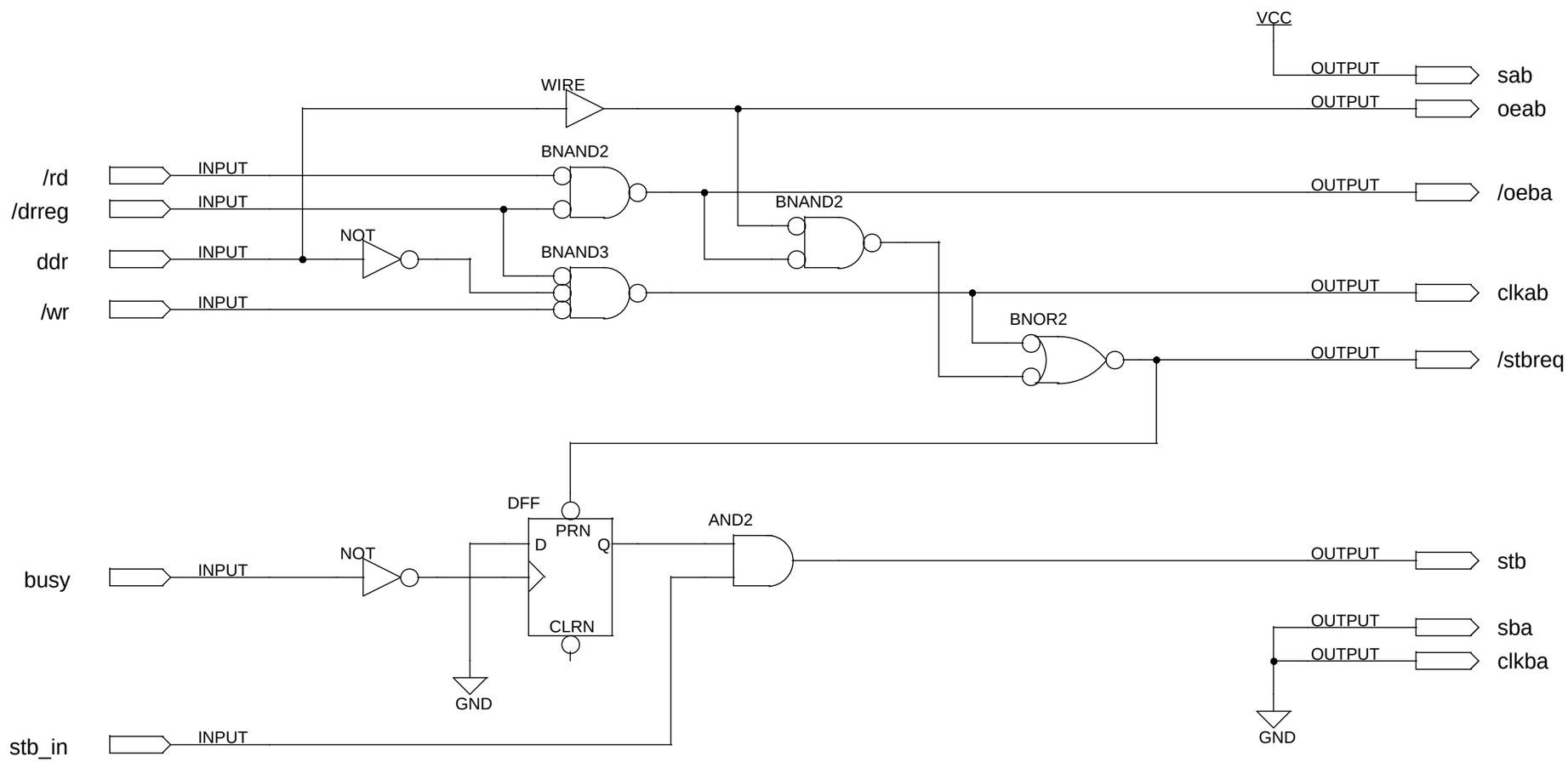
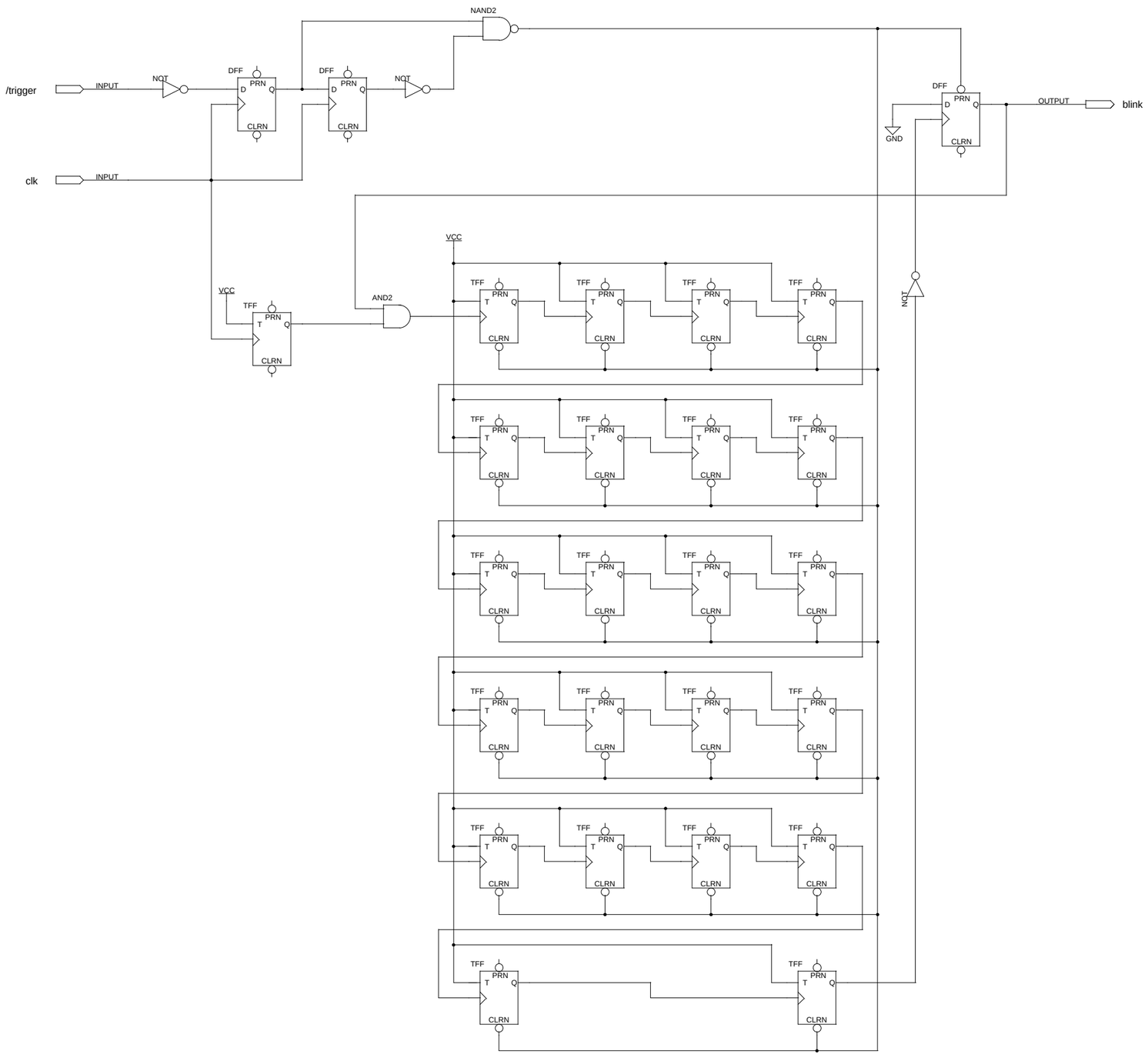

Bus reset
/rst
mr
/mr
clk
Keep the adrs latches always open
/cycle
/dmac
BA[15..0]
/bdsel
Enables data xcvrs
Lights the blue light
/select
not_here
Sets xcvr direction
r/w
/rd
/wr
noreg
reg
/idreg
/testreg
/k0reg
/k1reg
/ddrreg
/dr0reg
/dr1reg
/dr2reg
/dr3reg
/dr4reg
/dr5reg
/dr6reg
/dr7reg
/drsel
3:8 DECODER
Address-only decodes.
Timing must be added at point-of-use.
Data Direction Register
Test Register
74273b
OCTAL D-FF
dd[7..0]
ddr[7..0]
read_data[4][7..0]
test[7..0]
read_data[1][7..0]
Invalid register or bad address turns RDY on with no delay.
Delay before RDY on all valid register accesses, read and write.
Withhold RDY until done if BUSY from a previous operation.
obtctrl
stbgen
74164
SHIFT REG.
dirclk
busy
bd0
relay0
relay1
read_data[2][0]
read_data[2][7..1]
read_data[3][0]
read_data[3][7..1]
TP2
bd[7..0]
LPM_MUX
LPM_PIPELINE=
LPM_SIZE= 5
LPM_WIDTH=8
LPM_WIDTHS=CEIL(LOG2(LPM_SIZE))
read_data[0][7..0]
read_data[1][7..0]
read_data[2][7..0]
read_data[3][7..0]
read_data[4][7..0]
read_data[4..0][7..0]
ba[2..0]
dir3
dir2
dir1
dir0
Latch DIRx so that it can be validated
by STB
High data bus is used only for ID output
Low ID byte is muxed with other on-chip registers
bd[15..8]
High byte is module ID = 0x4E
Low ID byte is module revision = 0x01
Module ID = 0x4E01
0x00 is driven onto the high byte anytime the board is selected.
/rdy
read_data[0][7..1]
read_data[0][0]
DEVICE=EPM3256AQC208-7
2:08p 3-15-2005
1.00
Tom Zuchnik
Fermilab
HRM Decode for Rev D Digio



TITLE	HRM IO IO PORT CONTROL		
COMPANY	Fermilab		
DESIGNER	Tom Zuchnik		
SIZE B	NUMBER 1.00	REV A	
DATE 3:49p 6-23-2004		SHEET 1	OF 1



TITLE	HRM IO ONE-SHOT		
COMPANY	Fermilab		
DESIGNER	Tom Zuchnik		
SIZE D	NUMBER 1.00	REV A	
DATE 1:52p 9-16-2004		SHEET 1	OF 1