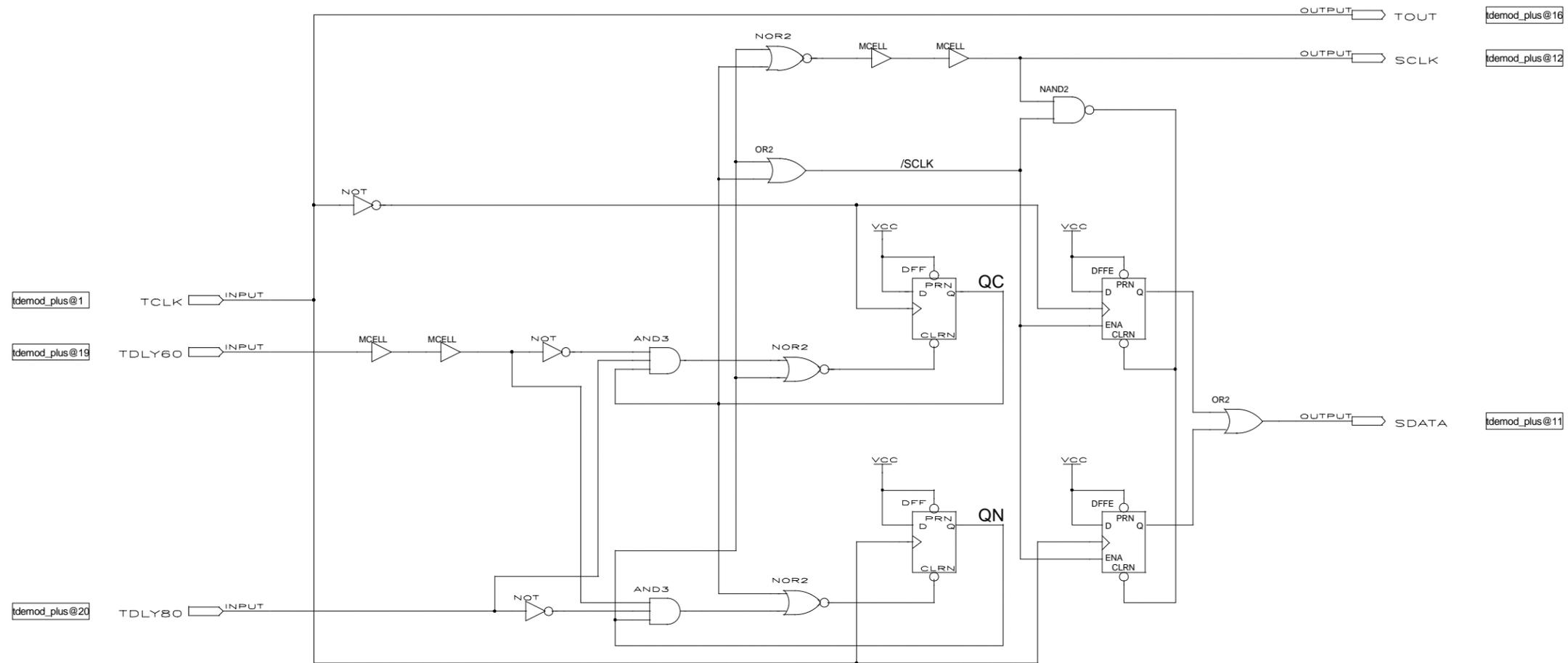


difaz_rx.gdf
3/27/01 0006 0977

TITLE				Diphase Receiver			
COMPANY				Fermilab			
DESIGNER				Paul Kasley			
SIZE	C	NUMBER	1.00	REV	A		
DATE	1:40p 3-27-2001			SHEET	1	OF	1



TDEMOM_PLUS.GDF

1. QN is set by L>H of TCLK. QC is set by H>L of TCLK.
2. QN is held reset by QC high. QC is held reset by QN high.
3. QN is reset 60-70ns after it is set by TCLK L>H. QC is reset 60-70ns after it is set by TCLK H>L.
One flop cannot be set while the other is set. TDLY60 must be longer than midbit to keep either flop from responding to a midbit transition.
4. The width of the reset pulse to QN and QC is determined by the prop delay loop from ANDgate-NORgate-flop-back to AND gate.
TDLY80 has nothing to do with circuit timing - it is used only to select which flop to reset. TDLY80 is used to "remember" if the cell boundary was L>H or H>L.
5. /SCLK enables the data flops to detect a mid-bit transition. The data flops are reset at the end of each bit cell by an ANDing of SCLK and /SCLK.
6. The MCELLs on TDLY60 allow for fine adjustment of the overall delay, since the next delay line tap is 80NS.
7. The MCELLs on SCLK are needed to generate the data reset and give some additional setup of SDATA relative to SCLK.

TITLE				TCLK DEMODULATOR			
COMPANY				Fermilab			
DESIGNER				PAK			
SIZE	D	NUMBER	1.00	REV	A		
DATE	1:24p	3-27-2001	SHEET	1	OF	1	