Fermilab

"New-New" Front Ends
NNSLD Command Reference

Issue E8, 9 Jan 2004, P. Kasley
Beams Division/Controls Group

Response Interrupts

The SLD generates a single response to each command it receives. The assertion of PCI INTA# is controlled by the host through the Interrupt Control and Status Register (INTCSR) in the AMCC S5933 PCI controller. PCI interrupt should be set up to trigger on AMBEF bit 30. See the S5933 data book for details.

The last operation done by the SLD in handling a command is a write to the high word of outbound mailbox 4 (OMBX4H). The INTCSR should be set up to trigger when the high word of mailbox 4 becomes full. The SLD then spins, waiting for ALL outgoing mailboxes to become empty. As soon as it sees this, the SLD returns to its normal poll loop and waits for a new command.

QXR Version:

The QXR 5760 Hz signal interrupts the processor through PCI INTB#. The processor must set the BIST bit in the AMCC S5933 configuration space register 0x4F, bit 6, to acknowledge INTB#. The QXR interrupt path is (almost) completely separate from the mailbox path and has no effect on standard operations. (Clearing INTB# at the PMC requires the use of a DSP interrupt. Servicing of the interrupt takes 250 ns and has the highest priority.)

TCLK Initialization

The TCLK FIFO should be initialized before use. Issue a TCLK Flush followed by a Mask All. Write to the mask RAM to enable specific events.

Watchdogs and Resets

The Rev. C NNSLD implements a hardware watchdog timer. However, the host software should periodically run a Loopback or Module Status command to check on the sanity of the NNSLD. There should also be a time limit on receiving a response to any NNSLD command. A hardware reset can be forced can be forced by writing a "1" to bit 24 of the S5933 MCSR from the PCI bus. This will also reset the DSP and force a re-load of the Altera gate array.

The DSP periodically checks the configuration status of the Altera FLEX device. This is done at one-half second intervals by reading specific fixed bit positions in two S5933 registers. If any of the bits are incorrect, a reload of the 10K30 is forced by the DSP and the DSP is reset. An "insanity count" is maintained at DSP data memory address 0x3F01. This location is incremented each time a FLEX reload occurs. Host software must initialize the value of the "insanity counter".

Command Chaining

Commands may be chained together for DMA access and processing by the SLD. The minimum length of a chain is 4 bytes (1 longword). The maximum length is 4092 bytes (1,023 longwords). Each command in a chain must have the chain byte set to $FF except that the last command in a chain must have the chain byte set to $00.

The PPC host must initialize the FIFO management bits in the NNSLD for chaining to work. These flags are in the INTCSR bits 24 through 31 and are not accessible from the DSP-side of the S5933 PCI controller. The contents are 31: “001011” :24. The host is responsible for setting up a PCI-addressable memory space in which lists are passed between the host and the SLD.

The chain flag is ignored in commands that are passed through the mailboxes. The CHAIN and RESET MODULE commands are ignored if they appear within a command chain.

Command List

0000	Loopback
0001	Enable Unsolicited TCLK
0002	Disable Unsolicited TCLK
0003	Set Flag
0004	Clear Flag
0005	Get Module Status
0006	Reset Module
0007	Send RD-CAMAC Message (Disabled in QXR version)
0008	Read ADSP2181 Data Memory
0009	Write ADSP2181 Data Memory
000A	Write DSP Code EEPROM
000B	BD CAMAC PIOX Operation
000C	Copy BTR Buffer from DSP to PCI
000D	Loopback
000E	QXR Set PGA Gain (Disabled in non-QXR version)
000F	Set CAMAC Mode/Manage BD-CAMAC Receivers
0010	Read TCLK Mask RAM, Page 0
0011	Read TCLK Mask RAM, Page 1
0012	Read TCLK Mask RAM, Page 2
0013	Read TCLK Mask RAM, Page 3
0014	Write TCLK Mask RAM, Page 0
0015	Write TCLK Mask RAM, Page 1
0016	Write TCLK Mask RAM, Page 2
0017	Write TCLK Mask RAM, Page 3
0018	Mask All TCLK Events
0019	Fetch TCLK Events
001A	Unsolicited TCLK Event Message
001B	Flush and Reset TCLK Receiver
001C	Chain
001D	Read Time
001E	Set MDAT Type Code
001F	Read MDAT Frame
0020	CAMAC Block Transfer Complete

SLD Commands

Note: The command must be the last word written to the inbound mailboxes from the PCI bus.

COMMAND: 0000
NAME: Loopback message
DESCRIPTION: The command and the accompanying message are copied from the SLD inbound mailboxes (PCI -> SLD) to the outbound mailboxes (SLD->PCI).
FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Message 3	Message 2	Message 1	Message 0

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Message 7	Message 6	Message 5	Message 4

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	Message 11	Message 10	Message 9	Message 8

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	00

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Message 3	Message 2	Message 1	Message 0

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Message 7	Message 6	Message 5	Message 4

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	Message 11	Message 10	Message 9	Message 8

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	00

COMMAND: 0001
NAME: Enable unsolicited TCLK event messages
DESCRIPTION: Response type 1A is generated whenever a TCLK event is received.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	01

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	01

COMMAND: 0002
NAME: Disable unsolicited TCLK event messages
DESCRIPTION: Response type 1A is disabled.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	02

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	02

COMMAND: 0003
NAME: Set flag
DESCRIPTION: Sets the flag bit
NOTE: THE FLAG BIT MUST BE SET BEFORE A “Write DSP Code Memory” COMMAND (000A) IS ISSUED

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	03

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	03

COMMAND: 0004
NAME: Reset flag
DESCRIPTION: Clears the flag bit

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	04

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	04

COMMAND: 0005
NAME: Get Module Status
DESCRIPTION: Module status and version information is returned.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	05

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	00	00	Status	Status

Status
0: Response 001A enabled
1: Flag
2-10: x
11: TCLK FIFO Overflow
12: Crate fan status
13: TCLK carrier detect
14: TCLK Latched FIFO Full (clocked by TCLK RREQ)
15: TCLK FIFO empty

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	DSP Sw. Major	DSP Sw. Minor	PCB Assy Vers.	PCB Vers.

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	00	00	10K30 Major	10K30 Minor

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	05

Firmware build of 9/18/98: DSP=C0, Assy=A, PCB=C, POF=B0. POF CRC=0153177B.
Firmware build of 2/4/99: DSP=C1 00053887, Assy=B, PCB=C, POF=C1, CRC=015478B1.
Firmware build of 11/10/99: DSP=C2 00054EAB, Assy=B, PCB=C, POF=C1, CRC=015478B1.
Firmware build of 11/03/99: DSP=C3 00056B22, Assy=B, PCB=C, POF=C2, CRC=0154D1D5.
For QXR Firmware build of 2/15/99: DSP=Q1, Assy=B, PCB=C, POF=Q1. POF CRC=?.
Firmware build of 2/5/02: DSP=C5 00058FDA, Assy=B, PCB=C, POF=C3 CRC=0154EB83.

COMMAND: 0006
NAME: Reset module
DESCRIPTION: The DSP, CAMAC, and TCLK are reset. The 10K30 is not reconfigured. This is a “soft reset”. A “hard reset” can be forced by writing a “1” to bit 24 of the MCSR.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	00	06

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	06

COMMAND: 0007
NAME: Send CAMAC
DESCRIPTION: Perform a single Beamline CAMAC XD-RD transaction **(Disabled in QXR version)**

FORMAT:
Inbound

MBX1 Byte 3	Byte 2	Byte 1	Byte 0
CAMAC Address	CAMAC Address	CAMAC Address	CAMAC Address

0: MC (MultiCrate)
When set, this bit allows one CAMAC operation to be seen by all the crates in a string. Not used in Epicure.
1-8: Crate number
9-13: Function
14-15: Branch
00=Meson, 01=Neutrino, 10=Proton

MBX2 Byte 3	Byte 2	Byte 1	Byte 0
Reserved, 00	CAMAC Control	CAMAC Control	CAMAC Address

0-3: Sub-address
4-8: Slot number
9: GL (Graded LAM)
"Not used. Included for compatibility with other systems that did not use it."
10: Z (Initialize)
Causes a dataway Z operation at the addressed crate. The CAMAC function sent with it is ignored.
11: L (Lock)
When set, the SLD will hold the linkmux grant for the next operation. The lock bit is forwarded to the addressed crate to locally secure crate access. This is used for atomic operations to modules.
12: Q (no-Q retries at crate controller)
When set, the crate controller is enabled to retry locally.
13-15: Always one
16-19: SLD no-Q retries
Number of times that the SLD will retry an operation before it returns a no-Q response.

MBX3 Byte 3	Byte 2	Byte 1	Byte 0
Reserved, 00	Write Data 16-23	Write Data 8-15	Write Data 0-7

MBX4 Byte 3	Byte 2	Byte 1	Byte 0
00	Chain	00	07

0007, Send CAMAC continued

Outbound

MBX1 Byte 3	Byte 2	Byte 1	Byte 0
Termination Flags	Reserved, 00	CAMAC Response	CAMAC Response

Note: The SLD does not check the return parity bits

CAMAC Response
0: 1
1: SP (Status Parity, odd)
2: E (the transmitted data contained a parity Error)
3: CL (crate off-Line)
4: X (X-response)
5: D (crate Demand)
6: Q (Q-response)
7: I (dataway Inhibit status)
8: 1
9: DP (read Data Parity, odd)

Termination Flags
24: NO_GNT (no grant received from link mux)
25: NO_Q (no Q was returned)
26: NO_ANSWER (the operation to the addressed crate timed out)

MBX2 Byte 3	Byte 2	Byte 1	Byte 0
Timestamp, byte 1	Timestamp, byte 0	Timestamp, byte 2	Reserved, 00

Timestamp is in units of 10usec. Maximum value is 168 sec. The value will saturate to 0xFFFFFF.

MBX3 Byte 3	Byte 2	Byte 1	Byte 0
00	Read Data 16-23	Read Data 8-15	Read Data 0-7

MBX4 Byte 3	Byte 2	Byte 1	Byte 0
X	00	00	07

COMMAND: 0008
NAME: Read ADSP2181 Data Memory
DESCRIPTION: Reads a 6 word block of DM

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	High DM adrs	Low DM adrs

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	08

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Word 1H	Word 1L	Word 0H	Word 0L

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Word 3H	Word 3L	Word 2H	Word 2L

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	Word 5H	Word 5L	Word 4H	Word 4L

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	08

COMMAND: 0009
NAME: Write ADSP2181 Data Memory
DESCRIPTION: Writes a word of DM

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Data H	Data L	High DM adrs	Low DM adrs

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	09

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	09

COMMAND: 000A
NAME: Write DSP Code Memory
DESCRIPTION: A pointer to a DSP code block in host memory is passed to the SLD. The SLD reads the data directly from host memory and writes it to the DSP boot memory. When finished, the SLD writes a response packet to the outbound mailboxes to notify the host that the operation is complete. The block length is fixed to 1,024 bytes (256 longwords).

The minimum length of a list is 4 bytes (1 longword). The maximum length is 4092 bytes (1023 longwords). The flag bit must be set for this command to execute. The flag bit is cleared when the command returns.
The address argument is truncated to the next lower longword value by the DSP.
This operation may take up to 100ms to complete.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	LA byte 3	LA byte 2	LA byte 1	LA byte 0

LA: 32 bit PCI-space address of the code block. The address must be on a longword boundary.

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	DSP BM Adrs byte 1	DSP BM Adrs byte 0

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

RA: 32 bit PCI-space address for the return list. The address must be on a longword boundary.

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	00	00	0A

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	Verify flag

Verify flag: $FFFF if the EEPROM data did not verify with the source data, $0000 if the command was successful, and $0001 if the flag bit was not set.

If the verify flag is set, programming should be retried. If the fault persists, the EEPROM may need to be physically replaced.

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Abort flag	X	X	X

Abort flag: $FFxx if an error occurred during a get or put DMA, $0000 otherwise

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	0A

COMMAND: 000B
NAME: BD CAMAC PIOX Operation
DESCRIPTION: Performs a single PIOX-PIOR CAMAC transaction.

For block transfers, the return data is buffered in DSP memory. Successive BTRs are concatenated in the buffer until the buffer is read using the "Copy BTR Buffer" command. Completion of a BTR triggers an asynchronous "CAMAC BLOCK TRANSFER COMPLETE" ($20) message.

FORMAT:
Inbound

MBX1 Byte 3	Byte 2	Byte 1	Byte 0
X	Retries	C	Flags

0-1: Operation Type: 00=Write, 01=Read, 10=BTR Setup, 11 undefined
2: x
3: Aggregate command
4: RNRB
5: RCRB
6: SNRA
7: SCRA
8-15: Crate address
16-23: Number of no-Q retries, 0-255

MBX2 Byte 3	Byte 2	Byte 1	Byte 0
BTR NAFH	BTR NAFL	PIOX NAFH	PIOX NAFL

<u>PIOX NAF</u>
0-4: Function
5: x
6-9: Sub-address
10: x
11-15: Slot

<u>BTR NAF</u>
16-20: Function
21: x
22-25: Sub-address
26: x
27-31: Slot

For block transfer, the PIOX NAF will always be N(24)F(16)A(15). The BTR NAF is used by the crate controller as the target address for the block transfer. Block transfers are always read-only.

MBX3 Byte 3	Byte 2	Byte 1	Byte 0
X	WRD or (WC-1)	WRD or (WC-1)	WRD or (NoQ-1)

WRite Data if CAMAC write operation or (Word Count-1) and (NoQ-1) retries if Block Transfer

MBX4 Byte 3	Byte 2	Byte 1	Byte 0
00	Chain	00	0B

Outbound

MBX1 Byte 3	Byte 2	Byte 1	Byte 0
Termination Flags	Status 3	Status 1	Status 2

Termination Flags
24: x
25: NO_Q
26: NO_ANSWER
27: CNAF mismatch
28: BTR buffer full
29: BTR busy
30: PIOR and BTR ignored
31: Aggregate command

MBX2 Byte 3	Byte 2	Byte 1	Byte 0
Frame 1 Flags	Timestamp, byte 2	Timestamp, byte 1	Timestamp, byte 0

MBX3 Byte 3	Byte 2	Byte 1	Byte 0
Frame 3 Flags	Data 16-23	Data 8-15	Data 0-7

MBX4 Byte 3	Byte 2	Byte 1	Byte 0
X	Frame 2 Flags	00	0B

Frame Flags
0: T1 (received frame parity)
1: T2
2: H1
3: H2
4: Frame parity error
5: Frame clock error
6,7: x

Termination Flags Explanation
No-Q: The addressed crate did not respond to a CNAF or the addressed module did not respond or the addressed crate controller did not accept a N24 CNAF
No-answer: The addressed crate did not respond to a CNAF
CNAF mismatch: The CNAF echo from the addressed crate did not match the transmitted CNAF
BTR busy: Set if a BTR is active when attempting a BTR operation
BTR buffer full: Set if BTR buffer is already full when setting up a BTR
Aggregate Command: The CNAF was sent as an aggregate command and no response is expected

The response packet is always updated, though one or more fields may be in error if any of the termination flags are set.

Block Transfer Behavior
A block transfer requires that a block transfer set-up be sent via PIOX to the target crate. If a BTR is already pending or if the return data buffer is full, an error is flagged and the set-up command is not transmitted. If the set-up command terminates with an error, the block transfer is cancelled. Note, however, that in the event of a CNAF mismatch error, it is possible that the target has received the BTR command and will return data even though the SLD has cancelled the BTR. The host needs to be able to deal with this possibility.

Once a BTR is set up, BTR is handled entirely by interrupts and there is no timeout enforced on BTR. The host should timeout the BTR and use the “0F” command to cancel an incomplete transfer.

Block transfer behavior is slightly different when the BTR is processed within a command chain. First, the “TRANSFER COMPLETE” messages are suppressed. Only a single message is queued, either after the chain is finished or after the last chained BTR is complete after the chain is finished. Second, the PIOX BTR set-up and the BTR itself must complete before the next command in the chain is processed. Again, no timeout is enforced by the SLD on the BTR. If a BTR hangs within a chain, the hardware watchdog will timeout and reset the SLD (see the “CHAIN” command).

COMMAND: 000C
NAME: Copy BTR Buffer from DSP to PCI
DESCRIPTION: Copies the Block Transfer Return buffer from DSP data memory to PCI memory. When the copy is finished, the DSP BTR pointer is reset to the first buffer location and the DSP buffer is cleared to zeros. The buffer is 16,384 bytes total capacity. Note that bus mastering must be enabled by the host processor via the INTCSR at S5933 register offset $38 for this command to complete successfully. A copy cannot be done while a BTR is active. A copy that is attempted with BTR BUSY has to be retried.

The BTR buffer will contain zero to many return blocks formatted as follows:

BTR setup word 1 (Retries, crate address, Flags)
BTR setup word 2 (BTR NAF, PIOX NAF)
BTR setup word 3 (BTR Word Count, BTR Retries)
BTR fifo status (D12=BTR receiver FIFO overflow)
Initial BTR control frame
0 to n BTR data frames
Second BTR control frame

FORMAT:

Inbound

MBX1 Byte 3	Byte 2	Byte 1	Byte 0
PCI adrs byte 3	PCI adrs byte 2	PCI adrs byte 1	PCI adrs byte 0

The PCI address must be on a longword boundary.

MBX2 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX3 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX4 Byte 3	Byte 2	Byte 1	Byte 0
00	Chain	00	0C

Outbound

MBX1 Byte 3	Byte 2	Byte 1	Byte 0
PCI adrs byte 3	PCI adrs byte 2	PCI adrs byte 1	PCI adrs byte 0

MBX2 Byte 3	Byte 2	Byte 1	Byte 0
Abort flag	X	Length byte 1	Length byte 0

Length: Return length in bytes, including the header words added by the NNSLD.
Abort flag: $FFxx if an error occurred during the DMA transfer, $0000 otherwise

MBX3 Byte 3	Byte 2	Byte 1	Byte 0
BTR	Busy	BTR Buffer	Overflow

Overflow: $FFFF for buffer overflow, $0000 otherwise
BTR Busy: $FFFF if BTR is in process on entry, $0000 otherwise

MBX4 Byte 3	Byte 2	Byte 1	Byte 0
X	00	00	0C

COMMAND: 000D
NAME: Loopback
DESCRIPTION:

FORMAT:

Inbound

MBX1 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX2 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX3 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX4 Byte 3	Byte 2	Byte 1	Byte 0
00	Chain	00	0D

Outbound

MBX1 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX2 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX3 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX4 Byte 3	Byte 2	Byte 1	Byte 0
X	00	00	0D

COMMAND: 000E
NAME: QXR Set PGA Gain
DESCRIPTION: Sets the four gain bits to the QXR PGA **(QXR Version Only)**

FORMAT:

Inbound

MBX1 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	PGA Gain

PGA Gain
3-0: ATT3-ATT0
7-4: x

MBX2 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX3 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX4 Byte 3	Byte 2	Byte 1	Byte 0
00	Chain	00	0E

Outbound

MBX1 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX2 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX3 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX4 Byte 3	Byte 2	Byte 1	Byte 0
X	00	00	0E

COMMAND: 000F
NAME: Set CAMAC Mode/Manage BD-CAMAC Receivers
DESCRIPTION: Set the SLD for Accelerator or Beamlines CAMAC format. Read PIOR and BTR status registers. Clear PIOR and BTR error-count registers. Reset PIOR and BTR receivers. Flush the BTR buffer.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Ignore	PIOR and BTR	X	Mode

Receivers are ignored when not zero

Mode	SLD Configuration
xxxx xx00	no change; read current configuration
xxxx xxx1	Accelerator
xxxx xx10	Beamlines

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Reset BTR	Err Count	Reset PIOR	Err Count

Non-zero value clears the count register AFTER status is read

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	Reset	BTR Rcvr	Reset	PIOR Rcvr

Non-zero value clears the receiver AFTER status is read.

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	0F

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Receiver Ignore	Status	X	Current Mode

The “Current Mode” field shows the mode AFTER the mode change is executed.

Mode	SLD Configuration
$01	Accelerator
$02	Beamlines

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	BTR status word H	BTR status word L	PIOR status word H	PIOR status word L

BTR Status Word Format	PIOR Status Word Format
0-11: error count	error count
13: FIFO full	FIFO full
14: FIFO empty	FIFO empty
15: BTR Active	x

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	0F

COMMAND: 0010
NAME: Read TeV Mask RAM, Events 00 through 3F
DESCRIPTION: The TCLK mask RAM is read. Mask bits for events 00 through 3F are returned. An event is masked by a “1” and enabled by a “0”.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	10

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Events 1F-18 Mask	Events 17-10 Mask	Events 0F-08 Mask	Events 07-00 Mask

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Events 3F-38 Mask	Events 37-30 Mask	Events 2F-28 Mask	Events 27-20 Mask

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	10

COMMAND: 0011
NAME: Read TeV Mask RAM, Events 40 through 7F
DESCRIPTION: The TCLK mask RAM is read. Mask bits for events 40 through 7F are returned. An event is masked by a “1” and enabled by a “0”.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	11

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Events 5F-58 Mask	Events 57-50 Mask	Events 4F-48 Mask	Events 47-40 Mask

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Events 7F-78 Mask	Events 77-70 Mask	Events 6F-68 Mask	Events 67-60 Mask

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	11

COMMAND: 0012
NAME: Read TeV Mask RAM, Events 80 through BF
DESCRIPTION: The TCLK mask RAM is read. Mask bits for events 80 through BF are returned. An event is masked by a “1” and enabled by a “0”.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	12

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Events 9F-98 Mask	Events 97-90 Mask	Events 8F-88 Mask	Events 87-80 Mask

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Events CF-C8 Mask	Events B7-B0 Mask	Events AF-A8 Mask	Events A7-A0 Mask

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	12

COMMAND: 0013
NAME: Read TeV Mask RAM, Events C0 through FF
DESCRIPTION: The TCLK mask RAM is read. Mask bits for events C0 through FF are returned. An event is masked by a “1” and enabled by a “0”.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	13

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Events DF-D8 Mask	Events D7-D0 Mask	Events CF-C8 Mask	Events C7-C0 Mask

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Events FF-F8 Mask	Events F7-F0 Mask	Events EF-E8 Mask	Events E7-E0 Mask

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	13

COMMAND: 0014
NAME: Write TeV Mask RAM, Events 00 through 3F
DESCRIPTION: Mask bits for events 00 through 3F are copied from the message to the TCLK Event Mask RAM. An event is masked by a “1” and enabled by a “0”.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Events 1F-18 Mask	Events 17-10 Mask	Events 0F-08 Mask	Events 07-00 Mask

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Events 3F-38 Mask	Events 37-30 Mask	Events 2F-28 Mask	Events 27-20 Mask

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	14

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	14

COMMAND: 0015
NAME: Write TeV Mask RAM, Events 40 through 7F
DESCRIPTION: Mask bits for events 40 through 7F are copied from the message to the TCLK Event Mask RAM. An event is masked by a “1” and enabled by a “0”.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Events 5F-58 Mask	Events 57-50 Mask	Events 4F-48 Mask	Events 47-40 Mask

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Events 7F-78 Mask	Events 77-70 Mask	Events 6F-68 Mask	Events 67-60 Mask

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	15

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	15

COMMAND: 0016
NAME: Write TeV Mask RAM, Events 80 through BF
DESCRIPTION: Mask bits for events 80 through BF are copied from the message to the TCLK Event Mask RAM. An event is masked by a “1” and enabled by a “0”.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Events 9F-98 Mask	Events 97-90 Mask	Events 8F-88 Mask	Events 87-80 Mask

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Events BF-B8 Mask	Events B7-B0 Mask	Events AF-A8 Mask	Events A7-A0 Mask

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	16

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	16

COMMAND: 0017
NAME: Write TeV Mask RAM, Events C0 through FF
DESCRIPTION: Mask bits for events C0 through FF are copied from the message to the TCLK Event Mask RAM. An event is masked by a “1” and enabled by a “0”.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Events DF-D8 Mask	Events D7-D0 Mask	Events CF-C8 Mask	Events C7-C0 Mask

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Events FF-F8 Mask	Events F7-F0 Mask	Events EF-E8 Mask	Events E7-E0 Mask

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	17

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	17

COMMAND: 0018
NAME: Mask all TeV Events
DESCRIPTION: Mask bits for events 00 through FF are set to 1.

FORMAT:

Inbound

MBX1 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX2 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX3 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX4 Byte 3	Byte 2	Byte 1	Byte 0
00	Chain	00	18

Outbound

MBX1 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX2 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX3 Byte 3	Byte 2	Byte 1	Byte 0
X	X	X	X

MBX4 Byte 3	Byte 2	Byte 1	Byte 0
X	00	00	18

COMMAND: 0019
NAME: Get 0 to 4 TeV events from the TCLK FIFO
DESCRIPTION: If there are clock events in the TCLK FIFO, up to four events are moved from the FIFO to the outbound mailboxes. Event 0 is the first event removed from the FIFO and Event 3 is the last event removed.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	19

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Event 1 Status	Event 1	Event 0 Status	Event 0

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Event 3 Status	Event 3	Event 2 Status	Event 2

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	Timestamp, byte 1	Timestamp, byte 0	Timestamp, byte 2	# of events, 0-4

Timestamp is in units of 10usec. Maximum value is 168 sec. The value will saturate to 0xFFFFFF.

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	19

Event N status:
0: Valid event
1-2: x
3: FIFO Overflow (unlatched FIFO full)
4: Fan status
5: TCLK carrier detect
6: TCLK Latched FIFO full
7: TCLK FIFO empty

COMMAND: 001A
NAME: Unsolicited TCLK event message
DESCRIPTION: A response message is placed into the outbound mailboxes when the TCLK FIFO contains one or more TeV events. Up to four events are moved from the FIFO to the outbound mailboxes. Event 0 is the first event removed from the FIFO and Event 3 is the last event removed.

If the SLD inbound mailbox receives a command field equal to $001A, the command will act exactly the same as command $0019.

FORMAT:
Inbound
(none)

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	Event 1 Status	Event 1	Event 0 Status	Event 0

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	Event 3 Status	Event 3	Event 2 Status	Event 2

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	Timestamp, byte 1	Timestamp, byte 0	Timestamp, byte 2	# of events, 0-4

Timestamp is in units of 10usec. Maximum value is 168 sec. The value will saturate to 0xFFFFFF.

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	1A

Event N status:
0: Valid event
1-2: x
3: FIFO Overflow (unlatched FIFO full)
4: Fan status
5: TCLK carrier detect
6: TCLK Latched FIFO full
7: TCLK FIFO empty

COMMAND: 001B
NAME: Flush and reset TCLK receiver
DESCRIPTION: The TCLK receiver is reset, the FIFO is flushed, and the mask ram is set.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	1B

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	1B

COMMAND: 001C
NAME: Chain
DESCRIPTION: A pointer to a list of commands in host memory is passed to the SLD. The SLD reads the list directly from host memory, executes the commands, and writes a list of responses directly into host memory. When finished, the SLD writes a response packet to the outbound mailboxes to notify the host that the list is complete.

The minimum length of a list is 4 bytes (1 longword). The maximum length is 4092 bytes (1023 longwords). The maximum length of any return list is the length of the command list passed to the SLD. List execution stops at the first command that has the chain flag set to zero or at the first command that fails. Note that when a chain fails, data that may have been placed into the BTR buffer during chain processing is not flushed.

The address and length arguments are truncated to the next lower longword value by the DSP.

The total execution time of a chain is limited by the hardware watchdog. The watchdog is strobed at the start of the chain. The chain must complete within about .5sec min (2.0 sec max) before the watchdog resets the SLD.

FORMAT:
Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	LA byte 3	LA byte 2	LA byte 1	LA byte 0

LA: 32 bit PCI-space address of the first command in the list. The address must be on a longword boundary.

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	LL byte 1	LL byte 0

LL: list length in bytes, 4 - 4092. The length must be evenly divisible by 4.

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	RA byte 3	RA byte 2	RA byte 1	RA byte 0

RA: 32 bit PCI-space address for the return list. The address must be on a longword boundary.

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	00	00	1C

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
LA byte 3		LA byte 2	LA byte 1	LA byte 0

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
Abort flag		X	RL byte 1	RL byte 0

RL: Return list length in bytes; always equal or less than LL
Abort flag: $FFxx if an error occurred during a get or put DMA, $0000 otherwise

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
RA byte 3		RA byte 2	RA byte 1	RA byte 0

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
X		00	00	1C

COMMAND: 001D
NAME: Read time
DESCRIPTION: The 32 bit timestamp counter is read. Each tick is 10 microseconds. The counter is reset by TCLK event $02.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	1D

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	time, byte 3	time, byte 2	time, byte 1	time, byte 0

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	1D

COMMAND: 001E
NAME: Set MDAT Type Code
DESCRIPTION: Sets the MDAT type code to select the frame received by the MDAT receiver.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	TC

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	1E

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	1E

COMMAND: 001F
NAME: Read MDAT frame
DESCRIPTION: The current content of the selected MDAT frame is returned.

FORMAT:

Inbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	00	Chain	00	1F

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	MDAT flag	Typecode	MDAT15-8	MDAT7-0

MDAT flag bit 7: cleared by a “Set Typecode” command and 125Hz, set by reception of a valid MDAT frame with correct type code. This bit will toggle if the frame is present. It will reset if a valid MDAT frame is not received or if the MDAT signal is lost.

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	00	00	1F

COMMAND: 0020
NAME: CAMAC Block Transfer Complete
DESCRIPTION: A response message is placed into the outbound mailboxes when a CAMAC Block Transfer completes.

If the SLD inbound mailbox receives a command field equal to $0020, the command will be processed as a loopback ($00).

FORMAT:
Inbound
(none)

Outbound

MBX1	Byte 3	Byte 2	Byte 1	Byte 0
	time, byte 3	time, byte 2	time, byte 1	time, byte 0

MBX2	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

MBX3	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	X	X

Timestamp is in units of 10usec.

MBX4	Byte 3	Byte 2	Byte 1	Byte 0
	X	X	00	20

Revision Information

Firmware build of 9/18/98: DSP=C0, Assy=A, PCB=C, POF=B0

Firmware build of 2/15/99: DSP=C1, Assy=B, PCB=C, POF=C1
ASSY: Added U21 74BCT245 for MDAT
DSP: Added MDAT commands
POF: Added MDAT receiver

QXR Firmware build of 10/24/03: DSP=Q1, Assy=B, PCB=C, POF=Q1
ASSY: Added U21 74BCT245 for MDAT
DSP: Added MDAT commands
POF: Added MDAT receiver

5 May 1999 Revision E1: Send CAMAC command, 07, correct branch for Proton is "10". Was "11".

10 Nov 1999 revision E2:
Module Status command, 05 DSP - firmware minor rev was C1.
BD CAMAC PIOX command, 0B - Added "BTR busy" termination flag and termination flags explanation

3 Nov 2000 Revision E3:
1. **Added CAMAC BTR Complete ($20) message**
2. **Added BTR status to "SET CAMAC MODE/MANAGE BD-CAMAC RECEIVERS" ($0F) command**
3. **Added BTR cancellation and cleanup on PIOX error**
4. **Corrected BTR handling within a command chain**
5. **Added full BTR reset to "SET CAMAC MODE/MANAGE BD-CAMAC RECEIVERS" command ($0F)**
6. **Some minor bug fixes**

Module Status command, 05 DSP - firmware minor rev was C2. POF minor rev was C1.

3 Apr 2001 Revision E4:
Command $0B: Corrected Inbound MBX3 BTR WC and NoQ values

14 May 2001 Revision E5:
Command $0C: Added BTR Busy

3 May 2002 Revision E6:
Added flag to ignore the PIOR and BTR receivers. When a crate starts jabbering due to a power glitch or a nearby lightning hit, the SLD gets overloaded. This provision allows the front-end to become deaf while it toggles all crate off-line bits to silence the jabbering crate. Changes affected commands $0B and $0F.

24 Oct 2003 Revision E7:
QXR changes:
Removed $0D, "QXR Request EVT37". EVT37 output on transition card is now TCLK event 35.
Revised QXR notes.

9 Jan 2004 Revision E8:
Updated note for revised QXR 5760Hz interrupt